824

CONTROLLING THREADING DISLOCATION DENSITIES IN Ge ON Si USING GRADEI LAYERS AND PLANARIZATION

Patent number: JP2000513507T

Publication date: 2000-10-10

Inventor:

Applicant:

Classification:

- international: H01L21/20

- european:

Application number: JP19990505004T 19980623

Priority number(s): WO1998US13076 19980623; US19970050602P 19970624; US19970059765P 19970916

Also published as:

WO985936

EP101612[illegible]

Abstract not available for JP2000513507T

Abstract of correspondent: **WO9859365**

A semiconductor structure including a semiconductor substrate (302), at least one first crystalline epitaxial layer (304) on the substrate, the first layer having a surface which is planarized, and at least one second crystalline epitaxial layer (306) on the at least one first layer. In another embodiment of the invention there is provided a semiconductor structure including a silicon substrate, and a GeSi (306, 308) graded region grown on the silicon substrate, compressive strain being incorporated in the graded region to offset the tensile strain that is incorporated during thermal processing. In yet another embodiment of the invention there is provided a semiconductor structure including a semiconductor substrate, a first layer having a graded region (304) grown on the substrate, compressive strain being incorporated in the graded region to offset the tensile strain that is incorporated during thermal processing, the first layer (304) having a surface which is planarized, and a second layer (306, 308) provided on the first layer.